IT IS CLAIMED:

1.   A method of maintaining a compressed count of a number of occurrences of an event that recurs during operation of an electronic system, comprising:

determining whether another event having a random or pseudo-random probability P of occurring in response to individual occurrences of said system event has occurred, and

updating a compressed count of the number of occurrences of said system event on those occasions when the randomly or pseudo-randomly occurring event has occurred.

2.   A method of maintaining a compressed count of a number of occurrences of an event that recurs during operation of an electronic system, comprising:

generating a random number upon individual occurrences of the event,

determining when a generated random number matches at least one predetermined value, and

in response to the generated random number matching said at least one predetermined value, updating a compressed count of the number of occurrences of the event within the electronic system.

3.   The method of claim 2, wherein said at least one predetermined value is one of N distinct values of random numbers that are possible to be generated, a maximum expected number M of events are permitted to occur in the electronic system, and the compressed count is maintainable up to at least a number equal to M divided by N.

4. The method of claim 2, additionally comprising seeding the random number generator upon initialization of the electronic system with a number generated by a second random number generator.

5. The method of claim 2, wherein determining when the generated random number matches said at least one predetermined value takes into account the number of said events that have cumulatively occurred in order to decrease a probability that the match will occur for an individual generated random number as the cumulative number of said events increases.

6. The method of any one of claims 2-5, wherein the method is carried out in an electronic system including non-volatile flash memory and the recurring event includes erasure of an addressed portion of the flash memory.

7. The method of claim 6, wherein both generating the random number and determining when the generated random number equals said at least one predetermined value occur during an individual erase voltage pulse applied to said addressed portion of the flash memory system.

8. A flash EEPROM system, comprising:

a plurality of blocks of non-volatile memory cells wherein the cells within individual ones of the blocks are simultaneously erasable,

a controller including a micro-processor that controls programming of data into addressed blocks of memory cells, reading data from addressed blocks of memory cells and erasing data from one or more of addressed blocks of memory cells at a time,

storage provided within the plurality of blocks of memory cells that maintains counts associated with individual ones of the memory cell blocks,

a number generator that randomly generates a number in response to one or more of the addressed blocks being erased, and

a comparator that causes at least one of the counts associated with one or more addressed blocks being erased to be updated when the generated random number matches a predetermined at least one of possible numbers generated by the random number generator.

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9.   The system of claim 8, wherein the number generator is characterized by generating one of a controlled total number of possible different random numbers, and wherein said total number of possible different random numbers is controlled by said at least one of the counts associated with one or more addressed blocks being erased.

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